Design and Analysis of 2 GHz Low Noise Amplifier Layout in 0.13um RF CMOS

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Abstract

This paper presents analysis of passive metal interconnection of the LNA block in CMOS integrated circuit. The performance of circuit is affected by the geometry of RF signal path. To investigate the effect of interconnection lines, a cascode LNA is designed, and circuit simulations with full-wave electromagnetic (EM) simulations are executed for different positions of a component. As the results, the position of an external capacitor \( (C_{ex}) \) changes the parasitic capacitance of electric coupling; the placement of component affects the circuit performance. This analysis of interconnection line is helpful to analyze the amount of electromagnetic coupling between the lines, and useful to choose the signal path in the layout design. The target of this work is the RF LNA enabling the seamless connection of wireless data network and the following standards have to be supported in multi-band (WCDMA: 2.11~2.17 GHz, CDMA200 1x : 1.84~1.87 GHz, WiBro : 2.3~2.4GHz) mobile application. This work has been simulated and verified by Cadence spectre RF tool and Ansoft HFSS. And also, this work has been implemented in a 0.13um RF CMOS technology process.

Keywords: cascode LNA (Low Noise Amplifier), RF CMOS, electromagnetic coupling, EM simulations, S-parameter

1. Introduction

The CMOS process is a good choice for current wireless communication systems due to advantages such as low cost and easy merging with digital block, so that CMOS process is widely used from digital circuit to millimeter wave circuits. Contrary to the millimeter wave circuit design as [1, 2], the relatively low RF circuit layout design operating in 1 to 5 GHz range is carried out without electromagnetic coupling consideration. However, the measurement result of fabricated CMOS circuit shows that the operating frequency goes down from the designed operating frequency. Even in the relatively low RF circuit, therefore, the electromagnetic coupling may be an issue that can affect the circuit performance.

The size of RF circuit is much smaller than its wavelength, so that the transmission line effects need not to be considered.
However, the electromagnetic coupling between the interconnection lines can be a critical factor depending on the location in the circuit. Moreover, as the scale-down is progressed in CMOS process, the electromagnetic coupling between interconnection lines will be increased. In this letter, the electromagnetic coupling between the passive metal interconnection structure of 2 GHz LNA is considered by full-wave EM simulation, and more accurate circuit layout design which is expected to be more similar to the real world can be achieved.

A simple crossed two metal line structure is shown in Figure 1. The structure has three layers of metal. The bottommost metal line (M1) act as ground planes, and the upper two metal lines (M5, M6) are used as signal lines. At the both ends of the signal lines, ports are assigned, so four ports exist. By full-wave EM simulation [3], S-parameter data between the ports is extracted, as shown in Table 1. The sum of the S-parameter column vector of each port (Port1:0.9962, Port2:0.9968, Port3:0.9961, Port 4:0.9971) is not unity. It can be assigned that some energy is radiated or dissipated. Moreover, comparing with Table 2, the elements of S-parameter have a numerical difference with each other. About one-tenth percent energy is coupled between signal metals. As the layout structure is more complicated, the inter-coupling effect degrades circuit performance much more.

![Figure 1. Designed cascode LNA structure.](image)

<table>
<thead>
<tr>
<th>S</th>
<th>Port1(Real/Imag)</th>
<th>Port2(Real/Imag)</th>
<th>Port3(Real/Imag)</th>
<th>Port4(Real/Imag)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port1</td>
<td>0.00112 -0.00930</td>
<td>0.99785 -0.02777</td>
<td>0.00043 0.00971</td>
<td>0.00043 0.01000</td>
</tr>
<tr>
<td>Port2</td>
<td>0.99758 -0.02777</td>
<td>0.00120 -0.00932</td>
<td>0.00043 0.01000</td>
<td>0.00044 0.00971</td>
</tr>
<tr>
<td>Port3</td>
<td>0.00043 0.00971</td>
<td>0.00043 0.01000</td>
<td>0.00143 -0.01170</td>
<td>0.99737 -0.03149</td>
</tr>
<tr>
<td>Port4</td>
<td>0.00043 0.01000</td>
<td>0.00044 0.00971</td>
<td>0.99737 -0.03149</td>
<td>0.00133 -0.01168</td>
</tr>
</tbody>
</table>
Table 2. S-parameter data at DC

<table>
<thead>
<tr>
<th>S</th>
<th>Port1(Real/Imag)</th>
<th>Port2(Real/Imag)</th>
<th>Port3(Real/Imag)</th>
<th>Port4(Real/Imag)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port1</td>
<td>0 0</td>
<td>1 0</td>
<td>0 0</td>
<td>0 0</td>
</tr>
<tr>
<td>Port2</td>
<td>1 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
</tr>
<tr>
<td>Port3</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>1 0</td>
</tr>
<tr>
<td>Port4</td>
<td>0 0</td>
<td>0 0</td>
<td>1 0</td>
<td>0 0</td>
</tr>
</tbody>
</table>

2 Related study

2.1 LNA structure

The LNA is designed for multi-band (WCDMA: 2.11~2.17 GHz, CDMA200 1x: 1.84~1.87 GHz, WiBro: 2.3~2.4GHz) mobile application. A well-known cascode LNA structure is adopted, and it is shown in Figure 1. M1 is a transconductance transistor which amplifies input signal, and M2 is a cascode transistor [4, 5] that suppresses Miller effect and improves reverse isolation. \(L_s\) is a source degeneration inductor, \(L_g\) is a gate inductor, and \(L_D\) is bias inductor and contributes to the output matching with \(C_L\). \(C_{ex}\) is an external capacitor that supplement \(C_{gs}\) to complete simultaneous noise and input matching [6].

\[
Z_{in} = sL_s + \frac{1}{sC_t} + \frac{g_m L_s}{C_t}
\]

\[
C_t = C_{gs} + C_{ex}.
\]

As can be seen from Eq. (1), \(Z_{in}\) represents the input impedance of the circuit [7]. The condition that allows simultaneously noise and input matching is shown in Eq.(2), and \(Z_{opt}\) denotes the optimum noise impedance [8, 9].

\[
Z_{opt} = Z_{in}^*.
\]

2.2 Full-wave electromagnetic (EM) simulation

The circuit is designed based on TSMC 0.13 um RF CMOS technology, and the designed layout is shown in Figure 2. The layout, which consists of one-poly and six-metal layers, can be analyzed by full-wave electromagnetic (EM) simulations with ANSOFT HFSS. The full-wave EM simulation analyzes more accurate effects of the electromagnetic coupling between interconnection lines of full layout. The result of full-wave EM simulation contains the information of self-parasitic RLC, coupling between the lines, and radiation in the chip. To analyze the electromagnetic coupling between the passive metal structures effectively [10], the active and the passive components are removed from the layout, and then the ports for measuring S-parameter of the passive interconnection lines are assigned at the position that was a connection between the component and the signal path. The positive port is connected to the signal path metal, and the negative port is connected to the nearest ground metal, and so there are 30 ports assigned, and the structure is put in a
dielectric box whose dielectric constant is four in order to take into account the effect of intermediate dielectric material. From the full-wave EM simulation, S-parameter of full layout is extracted, and the effect of electromagnetic coupling can be understood by comparing the S-parameter at the operating frequency with the S-parameter at DC condition. The extracted S-parameter can be included to the circuit simulation which is carried out by Cadence Spectre RF.

![Figure 2. Layout of designed LNA](image)

Figure 3 shows the configuration of circuit simulation with extracted S-parameter from full-wave EM simulations. The extracted S-parameter data is included in the n-port S-parameter block, and the each positive port of the block is connected to the component, all negative ports to the ground. By means of the above simulation method, the results are expected to become more accurate by involving electromagnetic coupling between interconnection lines of full layout.

![Figure 3. Circuit simulation configuration with extracted S-parameter from full-wave EM simulations](image)
3. Test procedure and condition

The result of the simulation which contains the extracted S-parameter is shown in Figure 4, and the line CKT means the result from the circuit simulation without full-wave EM simulation, and the line P1 and P2 show the results which contain the full-wave EM simulation for two different layout cases. S11 gives us the input reflection of the circuit, S21 the gain of the circuit. The S11 curve by EM simulation is not so sharp as that by circuit simulation without electromagnetic analysis, and shifted to the lower frequency about 10%, and the S21 curve by EM simulation is, also, shifted to the lower frequency and the gain is lowered by nearly 2 dB, because the circuit is modified by the various electromagnetic coupling between the passive interconnection lines in the layout. To investigate the effect of electromagnetic coupling between interconnection lines, as an example, we have simulated for two different cases (position P1 and position P2 in Figure 2) of interconnection line paths connected by an external capacitor C_{ex} using the above-mentioned full-wave EM simulation method. As can be seen from (1), C_{t} is concerned in input impedance Z_{in}, and C_{t} can be controlled by C_{ex}. In fact the value of an external capacitor C_{ex} and a gate-source capacitance C_{gs} is not so large (e.g. hundreds of femtofarad), and so simultaneous noise and input matching can be accomplished by external capacitor C_{ex}. Therefore the parasitic capacitance by electric coupling between the path L_{g}-C_{ex} and the path M1-C_{ex} may affect the circuit performance seriously.

When the external capacitor C_{ex} is on position 1, the path L_{g}-C_{ex} is shorter than the other case, so that the electromagnetic coupling between the path L_{g}-C_{ex} and the path M1-C_{ex} is reduced. Therefore, as the parasitic capacitance is smaller, S11 is less shifted to lower frequency than the other case, because the electric coupling between the path L_{g}-C_{ex} and the path M1-C_{ex} is less contributed to extra C_{ex}. The simulation results are shown in Fig. 4, the line P1 is less shifted to the lower frequency than the line P2. The amount of the coupling depends on the parallel length of those two lines, and can be estimated by observing the extracted S-parameter of these two passive interconnection lines in the layout.

There is no coupling between the ports at DC condition, as expected. In the results which involve full-wave EM simulations, however, there is quite an amount of electromagnetic coupling between the ports, as can be seen in Table 1. Port a and port b are assigned on the path L_{g}-C_{ex} and the path M1-C_{ex}, respectively, so that S_{ab} shows the amount of electromagnetic coupling between the path L_{g}-C_{ex} and the path M1-C_{ex}, and |S_{ab}| the absolute value of S_{ab}. The coupling between the lines is capacitively contributed to the external capacitor C_{ex} to lower the S-parameters of the circuit. As can be seen in Table 3, the amount of coupling between the lines when the external capacitor C_{ex} is on position 1, is smaller than that on position 2, because the parallel-line length of P1 is shorter than that of P2. Therefore the parasitic capacitance when the external capacitor C_{ex} is on position 2 is larger than the other P1 case. Therefore, when laying out in an RF circuit, it should be avoided to position the lines as parallel as possible and implemented in as short lines as possible. The amount of electromagnetic coupling between the path L_{g}-C_{ex} and the path M1-C_{ex} should be reduced by placing P1 and P2 close as shown in Figure 2.
Figure 4. S11 and S21 response of the circuit.

Table 3. S-parameter data of interconnection lines at 2 GHz

<table>
<thead>
<tr>
<th>S-parameter</th>
<th>At DC</th>
<th>Position 1</th>
<th>Position 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>S_{ab}</td>
<td>$</td>
<td>0</td>
</tr>
</tbody>
</table>

4 Conclusion

In this study, the full-wave EM simulation result is included in RF CMOS circuit layout design. The simulation results which take into account full-wave EM simulation results show that the operating frequency of the circuit is shifted to the lower frequency by nearly 10%, and the gain is reduced about 2 dB compared with the result of the circuit simulation without electromagnetic considerations. Moreover, depending on layout design, for example, the placement of external capacitor $C_{ex}$ in LNA design, the S11 and S21 are shifted to the lower frequency sensitively. Layout parasitic components can significantly affect the performance of CMOS RF integrated circuits, and can even make a totally different representation from the circuit designed in schematic. This paper proposes a fast approach to identify the layout effect based on S-parameter of on-chip interconnect structures extracted by 3D full-wave EM simulation. In order to confirm the accuracy of modeled on-chip passive devices used in the approach, S-parameter of interconnections is firstly computed at DC and compared with schematic simulation result. The results show that the effect of electromagnetic coupling between passive interconnection lines in RF CMOS process can affect the circuit performance seriously, and so the designer need to consider electromagnetic coupling in RF CMOS circuit layout design. Experimental results demonstrate that layout effect can be definitely non-negligible.
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References


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